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RAKE RECEIVER HAVING SEVERAL FINGERS AND METHOD OF PROCESSING AN INCIDENT SIGNAL THEREIN

PRIORITY CLAIM

The present application claims priority from French Application for Patent No. 02 12025, filed September 27, 2003, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to the processing of incident signals in a signal receiver.

Description of Related Art

[2] Receivers are known that combine several multi-path signal components mutually retarded by different time delays before reaching the receiver.

[3] For example, one such receiver is present in Code Division Multiple Access (CDMA) wireless communication systems, that experts in the subject usually call a "RAKE" receiver.

[4] In a wireless communication system, a base station communicates with several remote terminals such as mobile cell phones. Frequency Division Multiple Accesses (FDMA) and Time Division Multiple Accesses (TDMA) are traditional multiple access schemes to supply simultaneous services to a number of terminals. The basic idea on which the FDMA and TDMA systems are based is to share the available resource into several frequencies or several time slots respectively, such that several terminals can operate simultaneously without causing interference.

[5] Telephones operating according to the GSM standard belong to the FDMA and TDMA systems in the sense that transmission and reception take place at different frequencies and also at different slots.

[6] Unlike these systems that use a frequency division or a time division, CDMA (code division multiple access) systems enable multiple users to share a common frequency and a common timing channel, by using a coded modulation. CDMA systems include the CDMA 2000 system, the wide band CDMA (WCDMA) system, and the IS-95 standard.

[7] As is well known to an expert in the subject, a scrambling code is associated with each base station in CDMA systems to make a distinction between one base station and another. Furthermore, an orthogonal code known to an expert in the subject as the "OVSF (Orthogonal Variable Spreading Factor) code," is allocated to each remote terminal (for example like a mobile cell phone). All OVSF codes are orthogonal with each other, so that one channel can be distinguished from another.

[8] Before transmitting a signal on the transmission channel to a remote terminal, the signal is scrambled and spread by the base station using the scrambling code of the base station and the OVSF code of the channel.

[9] In CDMA systems, a distinction can still be made between systems that use a distinct frequency for transmission and for reception (CDMA-FDD system) and

systems that use a common frequency for transmission and reception, but have distinct time domains for transmission and reception (CDMA-TDD system).

[10] An incident signal, for example received by a mobile phone, comprises several versions of the initially transmitted signal with different time delays. These versions of the initial signal are the result of the multi-path transmission characteristics of the transmission medium between one base station and the telephone. It is recognized that each path introduces a different delay.

[11] The "RAKE" receiver installed in a mobile cell phone operating in a CDMA communication system is used to make the time alignment, descrambling, despreading, the channel correction and the combination of delayed versions of the initial signals, so as to deliver information flows (symbols) contained in the initial signals.

[12] All of these functions require the use of considerable memory means and/or a high operating frequency and large adders, particularly for the combination means of the receiver. The result is not only larger and more expensive equipment, but also higher power consumption.

SUMMARY OF THE INVENTION

[13] The present invention is advantageously applicable to CDMA type communication systems, and more particularly to WCDMA systems with terrestrial radio accesses (UTRA FDD/TDD).

[14] The present invention is intended to overcome the disadvantages of the prior art and its purpose is particularly to propose a combination of delayed versions of signals within a receiver, requiring a small memory and low operating frequency, and a single symbol size adder.

[15] Particularly in CDMA systems, symbols are transmitted within successive frames, each frame being subdivided into a number of slots. Each slot transports a number of symbols, each symbol being composed of a predetermined number of chips. The first symbol (the zero symbol) is received at the beginning of each slot. In accordance with the invention the Rake receiver operation is started at the beginning of the frame or slot, or during a frame or a slot.

[16] Another purpose of the invention is to facilitate addition and/or elimination of fingers, even during a frame or a slot. Therefore, the present invention proposes a

method of processing an incident signal within a "RAKE" receiver with several fingers, comprising reception of the incident signal formed of symbols output from at least one multi-path transmission channel for which each path transports a delayed version of the signal, detection of paths and allocation of these paths to at least some of the fingers, and a combination of the information output from each finger assigned to a path, within a memory means.

[17] According to one general characteristic of the invention, the memory means is capable of storing a number of symbols larger than the maximum delay between the paths (expressed as a number of symbols) and can be addressed by address pointers associated with the corresponding fingers.

[18] A first finger and a last finger are defined, in other words the finger that corresponds to the leading path and the finger that corresponds to the trailing path.

[19] The combination step then includes a steady state phase in which the address pointers point to addresses with mutual spacings taking account of mutual delays between the paths, and in which a current symbol received on a first finger is stored in the said memory at the write address

denoted by the corresponding address pointer, and this address pointer is then incremented.

[20] And before reception of the next symbol on this first finger, the contents of the memory stored at the read addresses denoted by all the other address pointers, are extracted in sequence, these contents are summed in sequence with the symbols present on the other fingers and, except for the sum corresponding to the last finger, then these sums are stored at the same read addresses before incrementing all the other pointers (including the pointer corresponding to the last finger).

[21] The last sum corresponding to the last finger is then delivered at the output from the receiver.

[22] The combination step also advantageously comprises a transient phase. And this transient phase is different depending on the case.

[23] Thus according to one embodiment of the invention, for example starting up the receiver at the beginning of the frame or slot, the combination step comprises a transient phase in which the initial addresses of the address pointers are all equal to the same initial value, for example zero, the different fingers output symbols

progressively and at corresponding different instants, and the same processing is done in this transient phase as is done in the steady state phase, and for the fingers on which the symbols are present.

[24] In other words, according to this embodiment, the fingers will progressively become "active" as they receive symbols, and the address pointers will progressively be incremented until the last finger has received a symbol. At this moment, the steady state phase will begin and the address pointers are mutually spaced by a number of symbols corresponding to the different delays between the paths.

[25] According to another embodiment of the invention, for example when the receiver is started during a frame or a slot, or when changing the configuration of the receiver during a frame or a slot, the combination step comprises a transient phase in which the initial addresses of the address pointers are predetermined taking account of any differences in the number of symbols between the paths.

[26] However, if exactly the same processing is done in the transient phase as in the steady state phase, in other words in particular the last sum corresponding to the last finger is delivered at the output from the receiver, then

information corresponding to incomplete combinations of symbols is output during this transient phase.

[27] This is why it is preferable to carry out the same processing in the transient phase as in the steady state phase, except for delivering the last sum corresponding to the last finger at the output from the receiver. In other words, no information is produced at the output from the receiver as long as the transient phase is not finished.

[28] According to one embodiment of the invention in which each symbol is composed of several chips, for example four chips, the rate of the combination step is controlled by a clock signal with a period equal to the duration of one chip divided by a predetermined number, usually a small number (for example equal to four in this case). The next step is to extract the memory contents denoted by a pointer during one cycle of the clock signal and the pointer corresponding to the next cycle is incremented.

[29] Normally, a memory has to be initialized before its contents can be read. Instead of doing this, the present invention advantageously avoids an additional write cycle by using a multiplexer that adds zero to the value of the symbol on the first finger before writing it in memory.

[30] According to one preferred embodiment of the invention, the number of symbols that can be stored in the memory means is equal to the number of symbols corresponding the maximum delay between paths, plus one symbol.

[31] Another purpose of the invention is to provide a "RAKE" receiver comprising:

a signal input to receive an incident signal formed from symbols output from at least one multi-path transmission channel in which each path transports a delayed version of the signal,

several fingers, each intended to demodulate a given path at a given instant,

a control unit designed to detect paths and allocate them to at least some of the fingers, and

a combination unit connected to the output from the fingers and designed to sum the information produced at the output from each finger.

[32] According to one general characteristic of the invention, the combination unit comprises:

a memory means capable of storing a number of symbols corresponding to the maximum delay between the paths,

address pointers associated with each corresponding finger, and

processing means with a steady state phase during which the address pointers point to addresses with mutual spacings taking account of the mutual delays between the paths, these processing means being capable of receiving a current symbol on a first finger during the steady state phase, storing it in the said memory at the write address given by the corresponding address pointer, and then incrementing the address pointer.

[33] Furthermore, the processing means can also perform the following steps in the steady state phase, before reception of the next symbol on the first finger,

read the contents of the memory stored at the read addresses denoted by the other address pointers, in sequence,

sum these contents with the corresponding symbols present on the other fingers, and then

store these sums, except for the sum corresponding to the last finger, at the same read addresses before incrementing the pointers,

the last sum corresponding to the last finger being delivered at the output from the combination unit.

[34] According to one embodiment of the invention, the processing means have a transient phase during which the initial addresses of the address pointers are all equal to the same initial value, for example zero, the different fingers delivering symbols progressively and at different instants, and the processing means are capable of performing the same processing during this transient phase as during the steady state phase, and for the fingers on which the symbols are present.

[35] According to one preferred embodiment of the invention, the processing means have a transient phase in which the initial addresses of the address pointers were predetermined taking account of offsets in the number of symbols between paths, and the processing means comprise inhibition means that are capable of preventing delivery of the last sum corresponding to the last finger at the output of the receiver during the transient phase.

[36] According to one embodiment of the invention in which each symbol is composed of several chips, the rate of the processing means is controlled by a clock signal with a period equal to the duration of one chip divided by a predetermined number (for example four) and the processing means extract the contents of the memory denoted by a pointer during one cycle of the clock signal and increment the corresponding pointer in the next cycle.

[37] Advantageously, the processing means comprise means of using the memory contents without the memory being initialized in advance. For example, this is done using a multiplexer by adding zero to the value of the symbol on the first finger before writing it in memory.

[38] According to one embodiment of the invention, in which each finger comprises several means of demodulating the transmission channels, several combination units are provided connected to the corresponding demodulation means of the different fingers.

[39] The receiver according to the invention is advantageously made in the form of an integrated circuit.

[40] Another purpose of the invention is a wireless communication system incorporating a receiver like that defined above.

[41] For example, this component may be a mobile cell phone.

BRIEF DESCRIPTION OF THE DRAWINGS

[42] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[43] FIGURE 1 diagrammatically illustrates a mobile cell phone according to the invention, incorporating a "RAKE" receiver according to the invention;

[44] FIGURES 2 to 4 diagrammatically illustrate the functions and an internal architecture of a "RAKE" receiver according to the invention;

[45] FIGURE 5 illustrates more details of an embodiment of a combination unit of a receiver according to the invention, used to implement the process according to the invention;

[46] FIGURE 6 shows a time diagram related to an embodiment of the process according to the invention;

[47] FIGURES 7a to 7l show an example of the variation of address pointers along the memory incorporated in the combination unit of the receiver according to the invention; and

[48] FIGURES 8a to 8f show another example of the variation of address pointers along the memory incorporated in the combination unit of the receiver according to the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[49] In FIGURE 1, the reference TP denotes a remote terminal such as a mobile cell phone that is in communication with a base station BS1, for example according to a CDMA-FDD type communication scheme.

[50] The mobile cell phone conventionally comprises an analog radio frequency stage ERF connected to an antenna ANT to receive an input signal ISG.

[51] Conventionally, the ERF stage comprises a low noise amplifier LNA and two processing channels comprising mixers, filters and conventional amplifiers (not shown in

FIGURE 2 for simplification reasons). The two mixers receive two signals with a phase difference of 90°, from a phase locked loop PLL. After frequency transposition in the mixers, the two processing channels define two flows, flow I (direct flow) and flow Q (data flow in quadrature), according to the nomenclature well known to an expert in the subject.

[52] After digital conversion in analog/digital converters, the two data flows I and Q are delivered to a reception processing stage ETNR.

[53] This processing stage ETNR comprises a receiver RR, commonly called a "RAKE receiver" by experts in the subject, followed by conventional demodulation means MP that demodulate the constellation delivered by the Rake receiver RR. The means MP are followed by a conventional channel decoder CD.

[54] Due to possible reflections of the initially transmitted signal on obstacles located between the base station and the mobile phone, the transmission medium is actually a multi-path transmission medium MPC, in other words comprising several different transmission paths (three transmission paths P1, P2, P3 are shown in FIGURE

1). Consequently, the signal ISG received by the mobile phone comprises different time delayed versions of the initially transmitted signal, versions that are the result of multi-path transmission characteristics of the transmission medium. And each path introduces a different delay. Obviously, the received signal ISG may also result from the transmission of initial signals transmitted by different base stations BS1 and BS2.

[55] FIGURE 2 diagrammatically illustrates the basic functions of the Rake receiver RR.

[56] This receiver is formed of several fingers (in this case N fingers) FG1 - FGN. Each finger is designed to demodulate a given received path at a given instant. Base band demodulation consists essentially of descrambling and despreading. Despreading is actually a correlation and consequently requires integration on the symbol period. The receiver then combines information received on each finger in the combination means MCMB, by summing them after correcting phase and amplitude distortions of each path (CHU unit described below). Obviously, the multiple fingers shown in figure 2 may be formed on the same

physical finger, reconfigured N times to make N functional fingers.

[57] The receiver also comprises a CHU unit capable of supplying a transmission channel estimate, particularly to correct channel distortions.

[58] The paths with the greatest energy have to be detected, and then allocated to fingers. This is done using an RMU control unit with a known structure.

[59] Finally, since the relative timing of paths can vary with time, a tracking unit (TU) with a known structure tracks the timing of the paths and updates the fingers with this information.

[60] FIGURE 3 shows that each finger FGi comprises a code generator CG capable in particular of producing scrambling codes and OVSF codes, an undersampler, actually a one-in-four undersampler placed at the input to the finger, and a channel estimating unit CHU.

[61] Furthermore, the finger FGi comprises several physical transmission channel demodulators, actually five demodulators DEM1 - DEM5. Each channel demodulator performs the descrambling, despreading and integration functions, and also the channel correction functions

mentioned above. The unit CHU is shared by all physical transmission channels.

[62] FIGURE 4 partially illustrates an example of an internal architecture of a RAKE receiver RR according to the invention, showing the receiver between the signal input ES and the output OP that delivers information about the different physical transmission channels (in this case five physical channels) and the fingers of the receiver, in this case six fingers FG1 - FG6, connected in output using MCMB combinations.

[63] In this case, these combination means MCMB are actually composed of one combination unit for each physical channel. One combination unit UCMB like that illustrated in FIGURE 5 and that will be described in more detail below, is actually connected to the five corresponding demodulators containing the six corresponding fingers FG1 to FG6.

[64] We will now more particularly refer to FIGURE 5 to describe one of these combination units UCMB, connected to the six demodulators of the six fingers all assigned to the same physical transmission channel.

[65] The duration of a chip in the case of an UTRA FDD system is 260.417 ns. Therefore, with a spreading factor of 4 (each symbol is formed from four chips), the duration of a symbol is of the order of 1.04 microseconds. According to this transmission standard, the maximum delay between fingers is very often of the order of about ten microseconds and in the worst case can be as high as 77 microseconds (296 chips) that corresponds to 74 symbols for a spreading factor of 4. In prior art, scanning of the complete window to detect any fingers would have required 74 processing operations between symbols, in other words one every 1.04 microseconds. The corresponding operating frequency is more than 70 MHz.

[66] However, the UCMB combination unit according to the invention is controlled by a clock signal CK with a period equal to the duration of a chip divided by 4 for a UTRA FDD system. In practice, the period of a clock signal is equal to 65.1042 ns corresponding to an operating frequency of 15.36 MHz.

[67] One of the elements of this combination unit UCMB consists of a memory MM capable of storing a number of

symbols equal to the number of symbols corresponding to the maximum delay between paths, plus one symbol.

[68] More precisely, if the maximum delay between the paths is 296 chips corresponding to 74 symbols for a spreading factor equal to four, the memory MM must then be capable of storing at least 74+1, in other words 75 symbols, in order to avoid loss of information. Thus in this case, a memory MM will be chosen capable of storing 75 symbols at the addresses that are deliberately indicated in a simplified form by numbers 0 to 74 in FIGURE 5.

[69] The unit UCMB also comprises processing means MT, comprising a multiplexer MUX1 at the input capable of receiving symbols SY1-SY6 on its six inputs, delivered successively by the corresponding six fingers of the receiver. This multiplexer MUX1 is controlled by a signal FGACT representative of the so-called "active" finger, in other words actually processed at a given instant.

[70] This signal FGACT is delivered by finger selection means FGSL. In this respect, each symbol present at the output from a finger is assigned a validity signal VFi. For example, a signal VFi equal to 1 means that the symbol

on the corresponding finger FGi is present, and that the finger may be considered as being an active finger.

[71] Each validity signal VFi is memorized in a flip-flop BSCi controlled by the clock signal CK and reset to 0 by a signal RSVi.

[72] As will be seen in more detail later, the function of these flip-flops is to memorize signals VFi until the processing means MT have processed the corresponding symbol.

[73] The selection means FGSL, in this case formed from six 2:1 multiplexers connected in series, and controlled by the corresponding flip flop outputs BSCi, will successively select the fingers considered as being active and will produce the control signal FGACT that will successively be set equal to the values of the active fingers so as to select the corresponding symbols.

[74] The receiver control unit RMU will also define which is the first finger of the receiver in other words which is the leading finger, and which is the last finger of the receiver, in other words the finger that will have the greatest delay, in each configuration. The first

finger is referenced in figure 5 by reference FF and the last finger is referenced by reference LF.

[75] The combination unit UCMB also comprises an adder ADD with the size of one symbol, controlled by the clock signal CK. This adder has a first input connected to the output from multiplexer MUX1 and a second input connected to the output from a second multiplexer MUX2.

[76] The output from the adder ADD is connected to the input of a demultiplexer MUX4 with two outputs.

[77] As can be seen in FIGURE 5, the multiplexer MUX2 has a first cabled input set to 0, and a second input to which the contents stored at a given address of the memory MM will be applied.

[78] This multiplexer MUX2 is controlled by a control signal SCM2 that is actually an output signal delivered by a comparator COMP1 that will compare the value of the signal FGACT with the value of the signal FF. In other words, the control signal SCM2 defines whether the finger that is active at a given instant is or is not the first finger.

[79] Similarly, a comparator COMP2 delivers a signal SCM1 defining whether the currently active finger is or is not the last finger.

[80] This signal SCM1 is applied to one of the inputs of an AND logical gate reference PL, and a control signal SCM4 that controls multiplexer MUX4 is applied to the output from this logical gate.

[81] Thus, depending on the value of this control signal SCM4, under steady state conditions the signal present at the input to the multiplexer MUX4 will either be delivered to the output OP from the combination unit UCMB, or written in the memory MM at the address defined by a current address pointer PTC.

[82] In this respect, a multiplexer MUX3, also controlled by the FGACT signal, will define which of the address pointers PTF1 - PTF6 associated with the six fingers of the receiver, will form the current address pointer PTC.

[83] Furthermore, incrementing means will be useful for incrementing the current pointer PTC by one unit, as will be seen in more detail later.

[84] The initial values of the address pointers PTFi, referenced PTF1IN - PTF6IN respectively, are predetermined and are fixed by the control unit RMU for each new configuration, and when a frame or a slot is in progress, take account of mutual differences in symbols between the different paths.

[85] In other situations, these initial values of pointers are identical and will for example be equal to 0, particularly when starting at the beginning of a frame or a slot.

[86] The logical gate PL forms part of the inhibition means MIB that will be reviewed again in further detail to describe the function.

[87] In this case, these inhibition means MIB comprise a register RGS initialized at the beginning of each configuration by the control unit RMU to the initial value PTFFIN of the address pointer for the first finger FF. This register may or may not be incremented by one unit as a function of the output signal SCM4 output by the logical gate PL.

[88] The inhibition means MIB also comprise a comparator COMP3 comparing the value of the current pointer PTC with

the value of a summation pointer PTS, that has the value contained in the register RGS.

[89] The output from the comparator COMP3 is applied to the other input of the logical gate PL.

[90] Furthermore, the processing means MT comprise transition detection means EDD with a conventional structure known in itself, to which the FGACT signal is applied and which delivers a signal FSCY representing a first cycle of the clock signal.

[91] These means EDD are followed by a flip-flop controlled by the clock signal CK and that outputs a signal SDCY representing the next cycle of the clock signal (second cycle).

[92] This flip-flop is itself followed by another flip-flop also controlled by the clock signal CK, the output of which produces the reset signal RSVi associated with the validation signal VFi of the finger FGi assumed to be active, during the third cycle of the clock signal.

[93] We will now describe an example operation of the combination unit UCMB in more detail, particularly with reference to FIGURES 5, 6 and 7a to 7l.

[94] As an example, in FIGURE 6 it is assumed that the six fingers are active and that finger No. 1 is the first finger, while finger No. 6 is the last finger.

[95] It can be seen in figure 6 that, as mentioned above, the corresponding validation signals SVFi output from the flip-flops are kept active as long as the symbol corresponding to the active finger at a given instant has not been completely processed by the processing means MT of the combination unit UCMB. The symbols are processed in series one after the other, beginning with the first finger and continuing until the last finger. A symbol is processed in two cycles of the clock signal, the signal to reset the active finger validation signal being output during the third cycle.

[96] Consequently, the six fingers are processed in twelve cycles, which leaves a margin of four cycles before the next symbols are applied to the corresponding fingers, if the spreading factor is equal to 4.

[97] In FIGURE 5, the number 100 denotes a step carried out for a finger considered to be active during the first cycle of the clock signal, while the number 200 denotes a

step carried out during the second cycle of the clock signal.

[98] In general, in the steady state phase, a current symbol received on a first finger is stored in the memory MM at the write address denoted by the corresponding address pointer (during the first cycle).

[99] This address pointer is then incremented (second cycle).

[100] And, before this next symbol is received on the first finger:

the contents of the memory stored at the read addresses denoted by all the other address pointers (first cycles), are extracted successively,

these contents are summed in turn with the symbols present on the other fingers (first cycles),

and these sums are then stored in sequence except for the sums corresponding to the last finger, at the same read addresses, before incrementing all the other pointers (second cycles),

the last sum corresponding to the last finger being delivered to the output from the receiver (during the second cycle).

[101] Obviously, incrementing the pointer after it has reached the address 74 will once again result in address 0.

[102] We will now illustrate more precisely this embodiment for a special case with particular reference to FIGURES 7a to 7l, corresponding to the combination unit being started during a slot, or a configuration being changed during a slot. In this respect, and for simplification purposes, it will be assumed that only three out of the six fingers, namely fingers 1, 2 and 3, are active in FIGURES 7a to 7l. Furthermore, it is also assumed that finger No. 1 is the first finger, while finger No. 3 is the last finger. Finally, it is assumed that the path associated with the second finger is delayed by two symbols with respect to the path associated with the first finger, while the path associated with the third finger is delayed by three symbols with respect to the path associated with the second finger. And the spreading factor is equal to 4.

[103] FIGURE 7a shows the initial values of the different address pointers. In this respect, it is assumed that the pointer PTF1 associated with finger No. 1 initially points

to address 5, while pointer PTF2 associated with finger No. 2 initially points to address 3 and pointer PTF3 associated with finger No. 3 initially points to address 0.

[104] The summation pointer PTS is initialized to the same address as the address corresponding to the initial value of the pointer for the first finger, in other words pointer PTF1.

[105] In FIGURE 7a, finger No. 1 is active. Consequently, during the first cycle of the clock signal, the current pointer PTC is equal to pointer PTF1 and points to address 5. On the other hand, the signal SCM2 output from the comparator COMP1 indicates that this finger is the first finger. Consequently, the output from the multiplexer MUX2 is equal to 0 and the adder ADD produces the symbol SY1 received on this first finger, on its output. Therefore, the multiplexer MUX2 is a means of starting from zero, although the contents of the memory located at address 5 is not necessarily equal to zero.

[106] On the other hand, the control signal SCM4 is equal to 0, since this finger does not correspond to the last finger. Consequently, during the second cycle of the clock signal, the symbol present on the first finger in the

memory MM is stored at the address pointed to by pointer PTF1, in other words address 5.

[107] Then, as illustrated in FIGURE 7b, the pointer PTF1 is incremented by one unit to make it point to address 6.

[108] Since the signal SCM4 is equal to 0, there is no need to increment the pointer PTS and it continues to point to the value 5.

[109] In the next cycle, in other words the third cycle (FIGURE 7c), the signal VF1 is reset to zero and this time the signal VF2 denotes the active finger (finger No. 2).

[110] The current pointer PTC is now the pointer PTF2, which points to address 3.

[111] Therefore during this third cycle, the contents of the memory located at address 3 are extracted and summed in the adder ADD with the symbol present on finger No. 2. Then during the fourth cycle (figure 7d), the sum thus obtained is stored at the address pointed to by pointer PTF2, which is always address 3, before incrementing the pointer PTF2 by one unit, which then points to the end of the second cycle at address 4.

[112] During the fifth cycle (FIGURE 7e), the pointer PTF3 will be the current pointer PTC. The memory contents

located at the address pointed to by pointer PTF3 are extracted and are summed with the symbol SY3.

[113] Many possibilities are then available. In general, there is no need to rewrite this sum in the memory since it is assumed to represent the symbol recombined with all components received on all the fingers. Normally, this sum is delivered to the output from the combination unit during the second cycle, under steady state conditions. But in this case, in other words when starting or restarting in the middle of a slot, and since the first finger has not changed to addresses less then five, the contents of the memory extracted during cycles three and five are not right, and this symbol cannot be used. In this case, according to the invention, these symbols can be lost since the impact is low.

[114] However, this symbol can be used if a simple multiplexer is used to reset the memory contents at the first access to each address.

[115] But in any case, if this sum is delivered during the fifth cycle, it will not represent a reconstituted signal since it would not take account of the contributions of fingers 1 and 2.

[116] This is why the invention advantageously does not deliver the sum that has been calculated at the output from the combination unit, since the transient phase is still active. This is the function of the inhibition means MIB. Although finger No. 3 is the last finger, the sum pointer PTS is not equal to the current point PTC. Consequently, the output from the logical gate P1 is still equal to 0, preventing the value delivered by the adder ADD from being delivered to the output OP.

[117] The pointer PTF3 is incremented during the sixth cycle (FIGURE 7f).

[118] We will now refer to FIGURE 7g that shows the situation in the seventeenth cycle, in other words when reading the next signal received on the first finger, for a spreading factor of four.

[119] In this case, the pointer PTF1 which is the current pointer, points to address 6. The operations carried out during this seventeenth cycle would be similar to those carried out during the first cycle.

[120] Then during the eighteenth cycle, after carrying out write operations comparable to the operations carried out during the second cycle, the value of the pointer PTF1

that now points to address 7 will be incremented by one unit (FIGURE 7h).

[121] In the twentieth cycle, the pointer PTF2 was incremented by one unit and now points to address 5 (FIGURE 7i).

[122] In the thirty-seventh cycle (FIGURE 7j), the current pointer is the pointer PTF3. However, the transient phase is still active, since the pointer PTF3 has not yet reached address 5, which is the address to which the pointer PTF1 was initially pointing. Consequently, there is still no information presented at the output from the combination unit.

[123] However, on the eighty-fifth cycle (FIGURE 7k), the current pointer is once again current pointer PTF3 that now points to address 5. The sum pointer PTS has not been incremented up to this point. At this moment, the current pointer PTC points to the same address as the sum pointer PTS. Moreover, since the pointer PTF3 is the pointer for the last finger, the two outputs from the logical gate PL are equal to 1, which means that the signal SCM4 will be set equal to the logical value 1.

[124] Consequently, the contents of the memory pointed to at address 5 can be delivered at the output from the combination unit. This marks the end of the transient phase and the beginning of the steady state condition. This information actually corresponds to reconstitution of a complete symbol that took account of contributions received on fingers 1, 2 and 3 respectively.

[125] In the next cycle (FIGURE 7l), the pointer PTF3 is incremented by one unit, now pointing to address 6. Similarly, the pointer PTS also points to address 6.

[126] In the future, the pointer PTS will track the pointer PTF3 so that when the third finger is active, the memory contents located at the address pointed at by this pointer PTF3 can be produced at the output from the combination unit.

[127] FIGURES 8a to 8f illustrate operation with a transient phase during which the symbols arrive progressively on the receiver fingers, for example when starting the combination unit at the beginning of a frame.

[128] In the example illustrated in FIGURES 8a to 8f, the first finger is finger No. 1 and the last finger is finger No. 3. Furthermore, finger No. 2 is delayed by one symbol

behind finger No. 1, and finger No. 3 is delayed by one symbol behind finger No. 2. The spreading factor is still equal to 4.

[129] In the first cycle (FIGURE 8a), the initial addresses of the pointers are identical and are equal to 0.

[130] Finger No. 1 is active in FIGURE 8a, and there is no other symbol present on the other fingers. Consequently, the current pointer PTC during the first cycle of the clock signal is equal to the pointer PTF1 and points to address 0. The adder ADD delivers the symbol SY1 received on this first finger, on its output.

[131] During the second cycle of the clock signal (FIGURE 8b), the symbol present on the first finger in the memory MM is stored at the address pointed to by pointer PTF1, in other words address 0.

[132] Then, as illustrated in FIGURE 8b, the pointer PTF1 is incremented by one unit so that it now points to address 1.

[133] Since no symbols were received on the other two fingers, the processing means will wait until the seventeenth cycle, in other words until reception of the

next symbol on finger No. 1, and a first symbol on finger No. 2.

[134] In the 17th cycle (FIGURE 8c), the pointer PTF1 that is the current pointer, points to address 1. The operations carried out during this seventeenth cycle will be similar to those carried out during the first cycle.

[135] In the 19th cycle, the pointer PTF2, which is the current pointer, points to address 0. During this nineteenth cycle, the operations carried out will be similar to the operations carried out during the seventeenth cycle, but for finger number two.

[136] In the thirty-third cycle (FIGURE 8d), the pointer PTF1, that is the current pointer, points to address 2. During this thirty-third cycle, the operations carried out will then be similar to the operations carried out during the first cycle. Note also that the pointer PTF2 was previously incremented by one unit and now points to address 1.

[137] In the 34th cycle (FIGURE 8e), the symbol on the first finger is stored in memory MM at the address pointed to by pointer PTF1, in other words to address 2, and the pointer PTF1 is incremented and now points to address 3.

[138] The same operations are carried out in the 35th and 36th cycles, for the second symbol on finger number two.

[139] In the 37th cycle (FIGURE 8f), there is a symbol present on the last finger. The memory contents located at address 0 pointed to by pointer PTF3 are extracted from memory and summed with the symbol present on the last finger.

[140] Furthermore, since the sum pointer PTS is equal to the current pointer that is the PTF3 pointer, this sum will be delivered to the output from the combination unit in the next cycle. And this sum actually corresponds to the recombination of the first symbol, for which the three contributions were received on the three fingers successively.

[141] The transient phase is then complete, and the next step is the steady state condition phase during which the address pointers will remain separated by an address corresponding to the mutual delays between the paths. As in the previous example, the pointer PTS will track the pointer PTF3, so that when the third finger is active, the memory contents located at the address pointed to by this

pointer PTF3 can be delivered at the output from the combination unit.

[142] Therefore, a smaller memory can be used, particularly due to the use of address pointers circulating along this memory. Instead of storing one value for each finger to make the sum later, the sum is calculated in real time, and all that is saved is this sum. Furthermore, an adder with the size of a symbol is all that is necessary.

[143] Furthermore, the frequency of the clock signal only depends on the number of cycles necessary to process all fingers and the duration of one symbol. This frequency is independent of the channel delay spread parameter representing the maximum delay between paths.

[144] Furthermore, although it is not essential, it is always possible to reset the contents of the memory located at the address pointed to by the address pointer of the finger that accesses this address before the others, at the time of arrival of a symbol on this finger.

[145] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing

Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.